REMARKS

The Examiner's Action mailed on December 8, 2008, has been received and its contents carefully considered.

In this Amendment, Applicants have amended the title of the invention, amended claims 1 and 2, and added new claims 3-7. Claim 1 is the sole independent claim, and claims 1-7 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

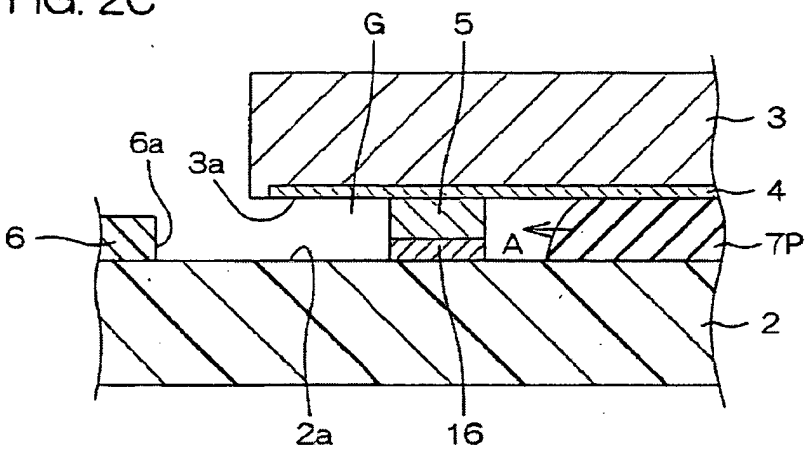
The title of the specification was objected to as non-descriptive, and has been amended accordingly. It is therefore respectfully requested that this objection be withdrawn.

Claims 1 and 2 were rejected under 35 USC §102(b) as anticipated by *Beddingfield et al.* (US 5,710,071). This rejection is respectfully traversed.

Claim 1 has been amended to recite "a pillar-shaped connecting member configured to connect the functional surface of the semiconductor chip to the surface of the solid state device". For support, see for example FIG. 2C and ¶[0028] of the present application:

ANNOTATED DRAWING

FIG. 2C



2	-	wiring board
2a	-	surface of wiring board
3	-	semiconductor chip
3a	-	functional surface of semiconductor chip
4	-	functional element
5	-	connecting member
6	-	solder resist film
6a	-	opening
7P	-	underfill material
16	-	connection pad
A	-	direction in which underfill spreads
G	-	gap

> **[0028]** Thereafter, the projection electrode **18** of the semiconductor chip **3** is positionally adjusted for the contact with a connection pad **16** of the substrate **15**, whereafter the bonding tool **19** is lowered so as to bond the semiconductor chip **3** with the substrate **15**. In this case, the semiconductor chip **3** is heated by the bonding tool **19**, and the solder material of the projection electrode **18** is melted by that heat, whereby the projection electrode **18** and the connection pad **16** are bonded together. *As a result, the connecting member **5** by which the substrate **15** and the semiconductor chip **3** are mechanically bonded together is formed. The wiring formed on the surface **15a** of the substrate **15** is electrically connected to the function element **4** of the semiconductor chip **3** by means of the connecting member **5**.*
>
> (emphasis added)

The Office Action alleges that "A semiconductor device, comprising: a solid state device; a semiconductor chip having a functional surface on which a functional element is formed" , as recited in claim 1, is disclosed in FIG. 5 and column 7, lines 23-28 of *Beddingfield et al.*, which reads "As illustrated in FIG. 5 and in accordance with an embodiment of the present invention, semiconductor die **20** is mounted on the wiring substrate such that hole **39** is located at or near the center of the semiconductor die. This is particularly important when wiring substrate **30** includes only one such hole **39**.".

The Office Action further alleges that "the semiconductor chip being bonded on a surface of the solid state device with the functional surface thereof facing the surface of the solid state device while maintaining a predetermined distance between the functional surface thereof and the surface of the solid state

device", as recited in claim 1, is disclosed in column 1, lines 21-25 of *Beddingfield et al.*, which reads "Because the conductive bumps making connections to the substrate are on the active surface of the die or chip, the die is mounted in a face-down manner, thus the name flip-chip".

The Office Action yet further alleges that "an insulating film provided on the surface of the solid state device facing the semiconductor chip, the insulating film having an opening greater in size than the semiconductor chip when the surface of the solid state device facing the semiconductor chip is vertically viewed down in plane", as also recited in originally filed claim 1, is disclosed in column 5, lines 42-51 thereof, which reads "As illustrated in FIG. 4, wiring substrate **30** also includes a solder mask **31** on the top and bottom surfaces of the substrate, selectively covering external conductive layers **37**. Solder masks are typically included on organic substrates, and not included on ceramic substrates. On the top surface, solder mask **31** includes an opening **41** for receiving a semiconductor die. Since the solder mask is made of an insulating material, portions of the wiring substrate which make electrical contact to the die must be exposed.", and that "a sealing layer that seals a space between the solid state device and the semiconductor chip", as further recited in claim 1, is disclosed in FIG. 12 and column 11, lines 64-65 thereof, which reads "An underfill encapsulation material **104** is then dispensed about the complete perimeter of the die array".

However, *Beddingfield et al.* fails to teach or suggest "a pillar-shaped connecting member configured to connect the functional surface of the semiconductor chip to the surface of the solid state device" as recited in amended claim 1.

The semiconductor device of *Beddingfield et al.* includes spherical conductive bumps **22**. Therefore, voids easily occur in narrow spaces between the conductive bumps and the wiring substrate **30** and between the conductive bumps and the die **20** when the semiconductor device is manufactured.

On the other hand, in the semiconductor device according to the invention, as recited in amended claim 1, such narrow spaces are not formed between the pillar-shaped connecting members and the solid state device and between the pillar-shaped connecting members and the semiconductor chip. Therefore, voids hardly occur around the pillar-shaped connecting members.

Thus, by employing "a pillar-shaped connecting member configured to connect the functional surface of the semiconductor chip to the surface of the solid state device", as recited in amended claim 1, the present invention overcomes the problem of voids occurring around spherical conductive bumps such as employed in *Beddingfield et al.*

Consequently, claim 1 patentably defines over *Beddingfield et al.* and is allowable, together with claims 2-7 that depend therefrom.

Newly added dependent claim 3 includes the feature that height of the connecting member (from the surface of the solid state device) is approximately equal to thickness of the insulating film. (See Fig. 2C of the present application). The space between the solid state device and the semiconductor chip is thus reduced so that the liquid sealing resin will rapidly enter the reduced space owing to marked capillarity.

Newly added dependent claim 4 includes the feature that the (pillar-shaped) connecting member is formed by bonding a connection pad provided on the solid state device and a projection electrode provided on the semiconductor chip. See ¶¶[0026] to [0028] in the specification of the present application:

> **[0001]** Thereafter, a semiconductor chip **3** having a projection electrode (bump) **18** connected to an electrode of a function element **4** is prepared. The projection electrode **18** includes a solder material.
>
> **[0002]** Thereafter, the substrate **15** is kept substantially horizontal while directing the surface **15a** thereof upward. The semiconductor chip **3** is held while the surface opposite the functional surface **3a** is being absorbed by a bonding tool **19** equipped with a heater for heating therein. The semiconductor chip **3** is caused to face the surface **15a** of the substrate **15** while directing the functional surface **3a** downward. FIG. 2A shows this state.
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> **[0003]** Thereafter, the projection electrode **18** of the semiconductor chip **3** is positionally adjusted for the contact with a connection pad **16** of the substrate **15**, whereafter the bonding tool **19** is lowered so as to bond the semiconductor chip **3** with the substrate **15**. In this case, the semiconductor chip **3** is heated by the bonding tool **19**, and the solder material of the projection electrode **18** is melted by that heat, whereby the projection electrode **18** and the connection pad **16** are bonded together. As a result, the connecting member **5** by which the substrate **15** and the semiconductor chip **3** are mechanically bonded together is formed. The wiring formed on the surface **15a** of the substrate **15** is electrically connected to the function element **4** of the semiconductor chip **3** by means of the connecting member **5**.

Newly added dependent claim 5 includes the feature that no other wiring than a connection pad for connection with the semiconductor chip is provided on the solid state device between the solid state device and the semiconductor chip. This corresponds to the embodiment shown in FIG. 3 in which the metallic balls **23** are re-wired only inside (not on the surface of) the wiring board **22a**. See ¶[0038] in the specification of the present application:

> **[0004]** In the wiring board **22**, metallic balls **23** are provided on an external connection surface **22b** opposite the surface **22a**. The metallic balls **23** are re-wired inside the wiring board **22** and/or on the surface of the wiring board **22**, and are electrically connected to a connecting member **5** on the side of the surface **22a**. The semiconductor device **21** can be bonded with other wiring boards (mounting boards) via the metallic balls **23**.

Newly added dependent claim 6 includes the feature that a distance between an outer periphery of the semiconductor chip and an edge of the opening of the insulating film is 0.1 mm or more when the surface of the solid state device facing the semiconductor chip is viewed from vertically above. See, for example, FIG. 1 and ¶¶[0012] and [0020] in the specification of the present application:

> **[0005]** Preferably, the distance between the outer periphery of the semiconductor chip and the edge of the opening of the insulating film is 0.1mm or more when the surface of the solid state device facing the semiconductor chip is vertically viewed down in plane.
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> **[0006]** The distance **D** between the outer periphery of the semiconductor chip **3** and the edge of the opening **6a** of the solder resist film **6** is set at 0.1mm or more when the surface **2a** is vertically viewed down in plane.

Newly added independent claim 7 includes the feature that the semiconductor chip is connected in a flip chip manner. See ¶[0001] in the specification of the present application:

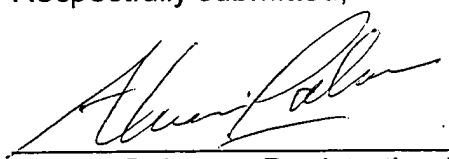
> **[0007]** This invention relates to a semiconductor device that has a semiconductor chip connected in a flip chip manner.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

No remittance is believed to be due. Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



February 27, 2009
Date

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